

# MCR8DSM, MCR8DSN

Preferred Device

## Sensitive Gate Silicon Controlled Rectifiers

### Reverse Blocking Thyristors

Designed for high volume, low cost, industrial and consumer applications such as motor control; process control; temperature, light and speed control.

- Small Size
- Passivated Die for Reliability and Uniformity
- Low Level Triggering and Holding Characteristics
- Available in Two Package Styles  
Surface Mount Lead Form — Case 369A  
Miniature Plastic Package — Straight Leads — Case 369
- Device Marking: Device Type, e.g., for MCR8DSM: CR8DSM, Date Code

#### MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage <sup>(1)</sup> (T <sub>J</sub> = -40 to 110°C, Sine Wave, 50 to 60 Hz, Gate Open) MCR8DSM MCR8DSN	V <sub>DRM</sub> , V <sub>RRM</sub>	600 800	Volts
On-State RMS Current (180° Conduction Angles; T <sub>C</sub> = 90°C)	I <sub>T(RMS)</sub>	8.0	Amps
Average On-State Current (180° Conduction Angles; T <sub>C</sub> = 90°C)	I <sub>T(AV)</sub>	5.1	Amps
Peak Non-Repetitive Surge Current (1/2 Cycle, Sine Wave, 60 Hz, T <sub>J</sub> = 110°C)	I <sub>TSM</sub>	90	Amps
Circuit Fusing Consideration (t = 8.3 msec)	I <sup>2</sup> t	34	A <sup>2</sup> sec
Forward Peak Gate Power (Pulse Width ≤ 10 μsec, T <sub>C</sub> = 90°C)	P <sub>GM</sub>	5.0	Watts
Forward Average Gate Power (t = 8.3 msec, T <sub>C</sub> = 90°C)	P <sub>G(AV)</sub>	0.5	Watt
Forward Peak Gate Current (Pulse Width ≤ 10 μsec, T <sub>C</sub> = 90°C)	I <sub>GM</sub>	2.0	Amps
Operating Junction Temperature Range	T <sub>J</sub>	-40 to 110	°C
Storage Temperature Range	T <sub>stg</sub>	-40 to 150	°C

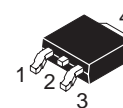
(1) V<sub>DRM</sub> and V<sub>RRM</sub> for all types can be applied on a continuous basis. Ratings apply for negative gate voltage; positive gate voltage shall not be applied concurrent with negative potential on the anode. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the device are exceeded.



ON Semiconductor

<http://onsemi.com>

SCRs  
8 AMPERES RMS  
600 thru 800 VOLTS



D-PAK  
CASE 369A  
STYLE 4

#### PIN ASSIGNMENT

Pin	Assignment
1	Cathode
2	Anode
3	Gate
4	Anode

#### ORDERING INFORMATION

Device	Package	Shipping
MCR8DSMT4	DPAK 369A	16mm Tape and Reel (2.5K/Reel)
MCR8DSNT4	DPAK 369A	16mm Tape and Reel (2.5K/Reel)

Preferred devices are recommended choices for future use and best overall value.

# MCR8DSM, MCR8DSN

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance — Junction to Case	$R_{\theta JC}$	2.2	$^{\circ}C/W$
— Junction to Ambient	$R_{\theta JA}$	88	
— Junction to Ambient <sup>(1)</sup>	$R_{\theta JA}$	80	
Maximum Lead Temperature for Soldering Purposes 1/8" from Case for 10 Seconds	$T_L$	260	$^{\circ}C$

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^{\circ}C$ unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
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## OFF CHARACTERISTICS

Peak Repetitive Forward or Reverse Blocking Current ( $V_{AK} = \text{Rated } V_{DRM} \text{ or } V_{RRM}; R_{GK} = 1.0 \text{ K}\Omega$ ) <sup>(2)</sup>	$I_{DRM}$ $I_{RRM}$	— —	— —	10 500	$\mu A$

## ON CHARACTERISTICS

Peak Reverse Gate Blocking Voltage ( $I_{GR} = 10 \mu A$ )	$V_{GRM}$	10	12.5	18	Volts
Peak Reverse Gate Blocking Current ( $V_{GR} = 10 \text{ V}$ )	$I_{RGM}$	—	—	1.2	$\mu A$
Peak Forward On-State Voltage <sup>(3)</sup> ( $I_{TM} = 16 \text{ A}$ )	$V_{TM}$	—	1.4	1.8	Volts
Gate Trigger Current (Continuous dc) <sup>(4)</sup> ( $V_D = 12 \text{ V}, R_L = 100 \Omega$ )	$I_{GT}$	5.0 —	12 —	200 300	$\mu A$
Gate Trigger Voltage (Continuous dc) <sup>(4)</sup> ( $V_D = 12 \text{ V}, R_L = 100 \Omega$ )	$V_{GT}$	0.45 — 0.2	0.65 —	1.0 1.5 —	Volts
Holding Current ( $V_D = 12 \text{ V}, \text{Initiating Current} = 200 \text{ mA}, \text{Gate Open}$ )	$I_H$	0.5 —	1.0 —	6.0 10	mA
Latching Current ( $V_D = 12 \text{ V}, I_G = 2.0 \text{ mA}$ )	$I_L$	0.5 —	1.0 —	6.0 10	mA
Total Turn-On Time (Source Voltage = 12 V, $R_S = 6.0 \text{ K}\Omega$ , $I_T = 16 \text{ A(pk)}$ , $R_{GK} = 1.0 \text{ K}\Omega$ ) ( $V_D = \text{Rated } V_{DRM}$ , Rise Time = 20 ns, Pulse Width = 10 $\mu s$ )	tgt	—	2.0	5.0	$\mu s$

## DYNAMIC CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit
Critical Rate of Rise of Off-State Voltage ( $V_D = 0.67 \times \text{Rated } V_{DRM}$ , Exponential Waveform, $R_{GK} = 1.0 \text{ K}\Omega$ , $T_J = 110^{\circ}C$ )	dv/dt	2.0	10	—	V/ $\mu s$

(1) Surface mounted on minimum recommended pad size.

(2) Ratings apply for negative gate voltage or  $R_{GK} = 1.0 \text{ K}\Omega$ . Devices shall not have a positive gate voltage concurrently with a negative voltage on the anode. Devices should not be tested with a constant current source for forward and reverse blocking capability such that the voltage applied exceeds the rated blocking voltage.

(3) Pulse Test; Pulse Width  $\leq 2.0 \text{ msec}$ , Duty Cycle  $\leq 2\%$ .

(4)  $R_{GK}$  current not included in measurements.

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## Voltage Current Characteristic of SCR

Symbol	Parameter
$V_{DRM}$	Peak Repetitive Off State Forward Voltage
$I_{DRM}$	Peak Forward Blocking Current
$V_{RRM}$	Peak Repetitive Off State Reverse Voltage
$I_{RRM}$	Peak Reverse Blocking Current
$V_{TM}$	Peak On State Voltage
$I_H$	Holding Current

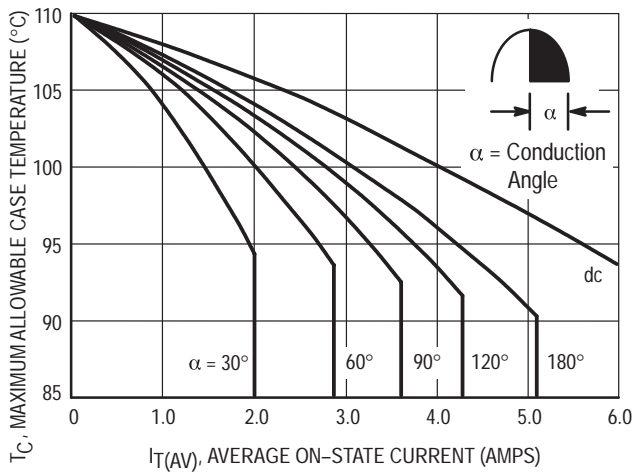
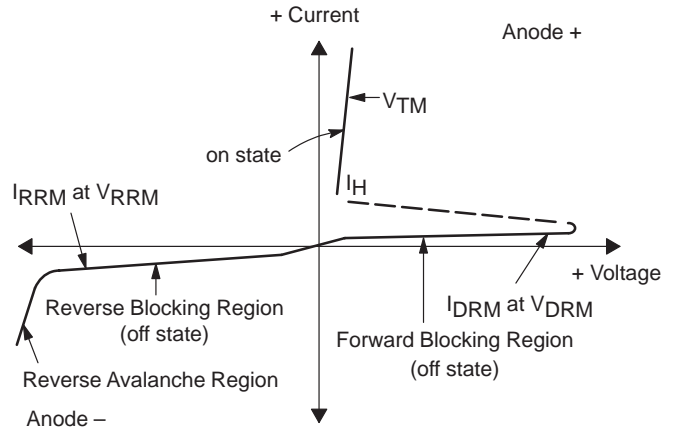


Figure 1. Average Current Derating

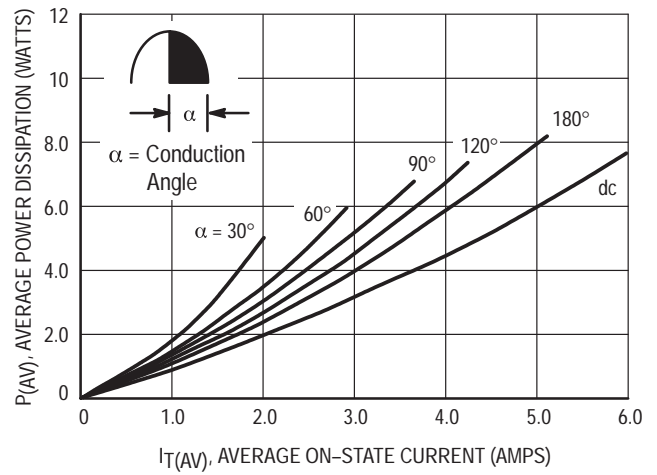


Figure 2. On-State Power Dissipation

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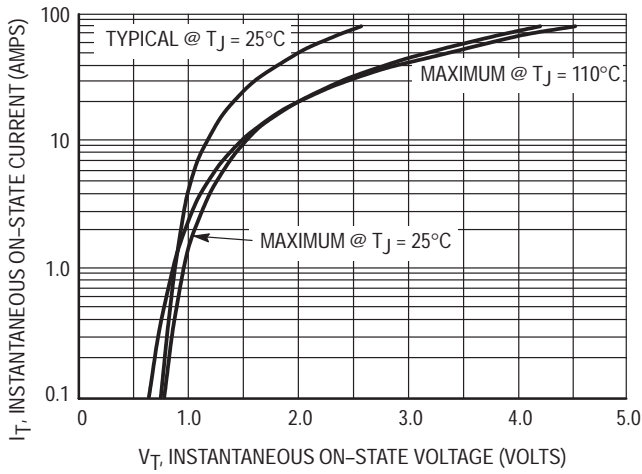


Figure 3. On-State Characteristics

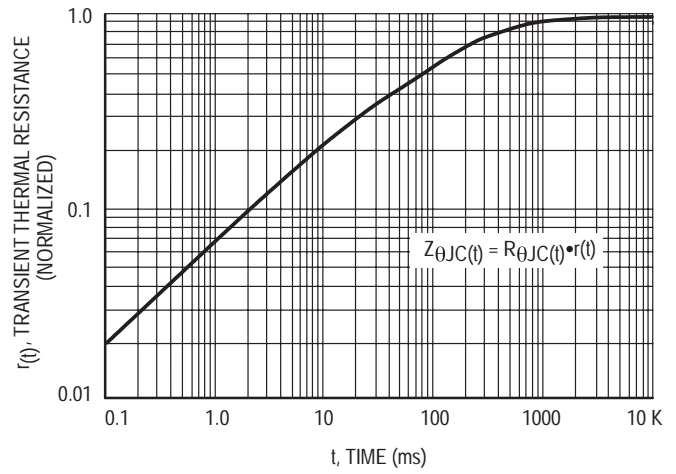


Figure 4. Transient Thermal Response

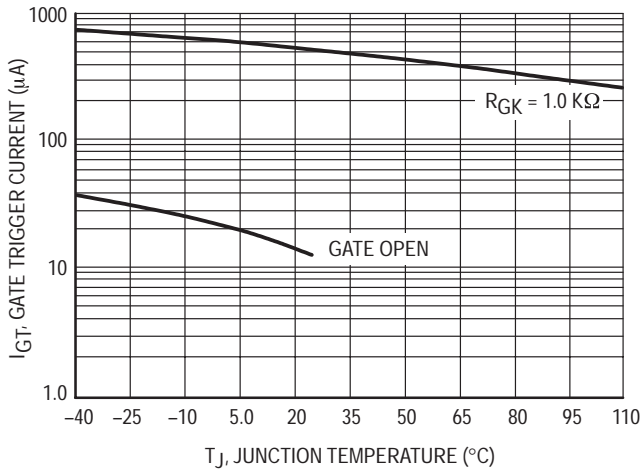


Figure 5. Typical Gate Trigger Current versus Junction Temperature

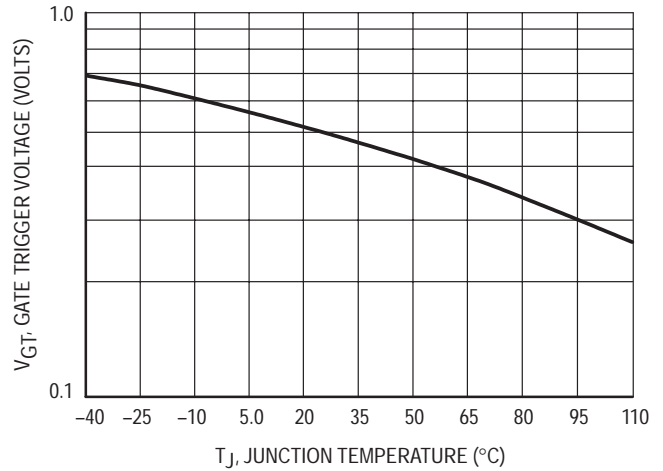


Figure 6. Typical Gate Trigger Voltage versus Junction Temperature

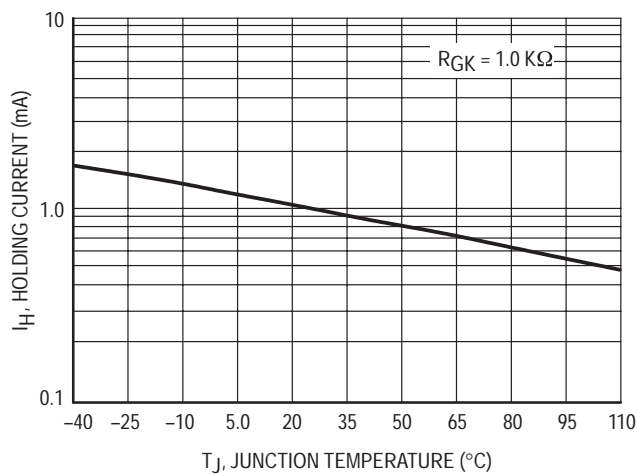


Figure 7. Typical Holding Current versus Junction Temperature

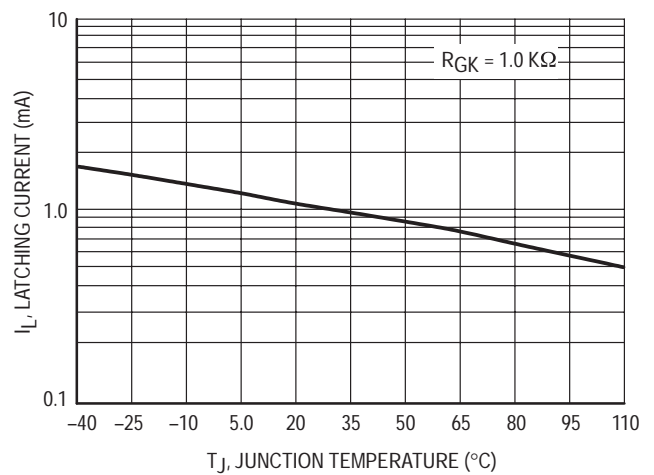
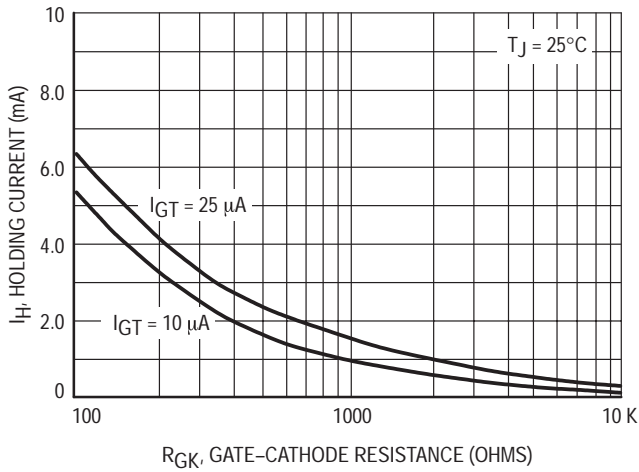
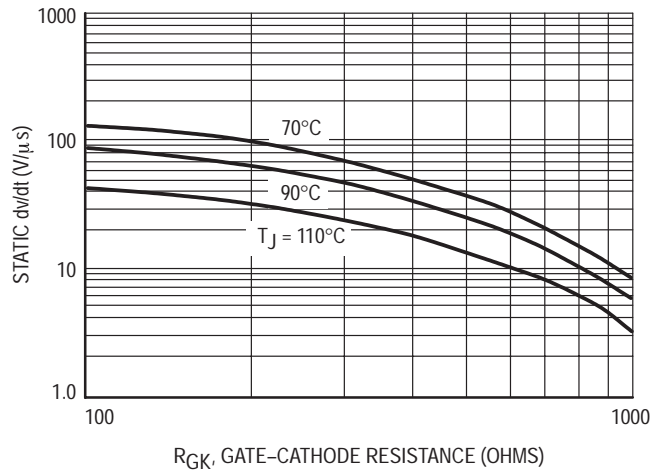


Figure 8. Typical Latching Current versus Junction Temperature

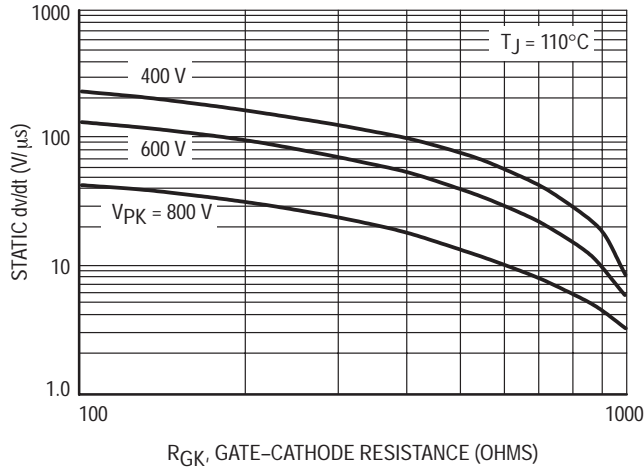
# MCR8DSM, MCR8DSN



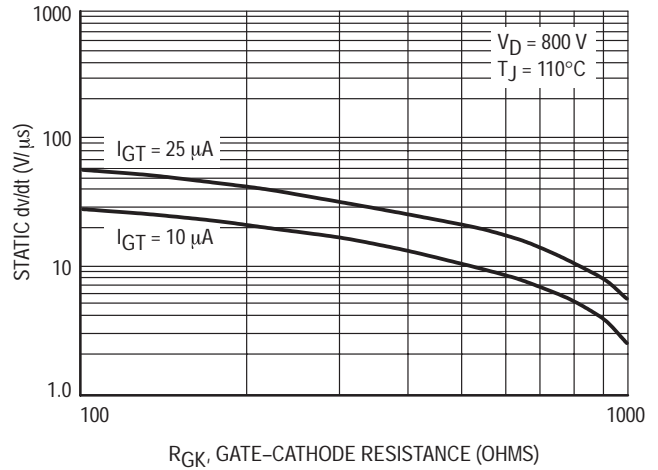
**Figure 9. Holding Current versus Gate-Cathode Resistance**



**Figure 10. Exponential Static  $dv/dt$  versus Gate-Cathode Resistance and Junction Temperature**



**Figure 11. Exponential Static  $dv/dt$  versus Gate-Cathode Resistance and Peak Voltage**



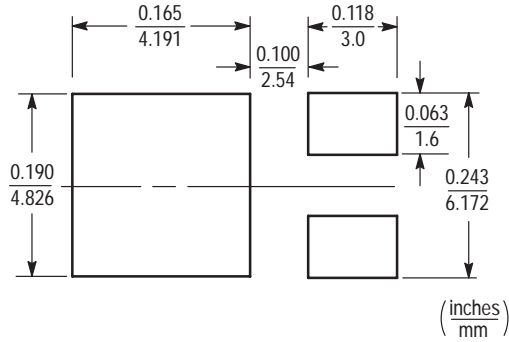
**Figure 12. Exponential Static  $dv/dt$  versus Gate-Cathode Resistance and Gate Trigger Current Sensitivity**

# MCR8DSM, MCR8DSN

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection

interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.

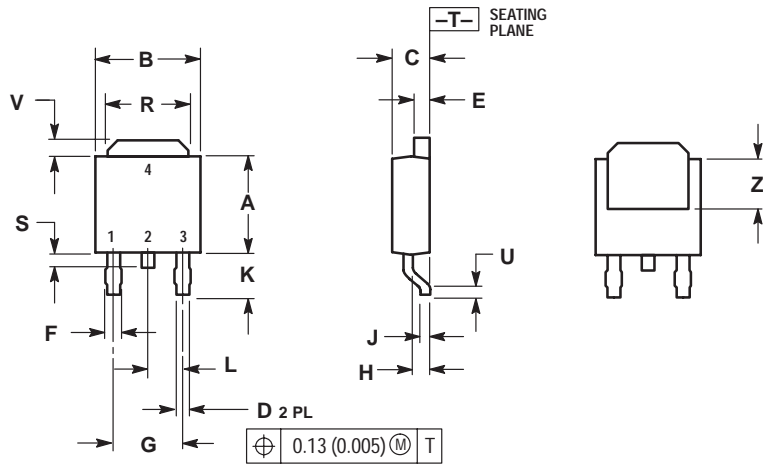


**DPAK**

# MCR8DSM, MCR8DSN

## PACKAGE DIMENSIONS

### D-PAK CASE 369A-13 ISSUE Z



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.250	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.033	0.040	0.84	1.01
F	0.037	0.047	0.94	1.19
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.175	0.215	4.45	5.46
S	0.020	0.050	0.51	1.27
U	0.020	---	0.51	---
V	0.030	0.050	0.77	1.27
Z	0.138	---	3.51	---

- STYLE 4:  
 PIN 1. CATHODE  
 2. ANODE  
 3. GATE  
 4. ANODE

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